

Addressing PCIe® Test and Debug Challenges with Confidence

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Agenda

- **Overview of PCIe® at 32GT/s**
- **PCIe Compliance Test & Challenges**
- **PCIe Automated Test Solutions**
- **Debugging Tools**

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Overview of PCIe at 32GT/s

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Early Pathfinding for 32GT/s

0.7 rev of Base Standard in place

- 32GT/s NRZ data rates and ~36dB channel loss at Nyquist, with no forward error correction
- 128/130b encoding, same as PCIe 3.0/4.0
- Typically 2 re-timers will be used in a 32GT/s link
- TS1/TS2 ordered sets in 8b/10b encoding as well as 128/130b encoding will be enhanced to include 32GT/s
- Equalization flows will be similar to PCIe 3.0/4.0
- EIEOS will be 32 consecutive ones followed by 32 consecutive zeros. Pattern length repeated for a total of 128UI.
- Compliance patterns will be identical to PCIe 4.0
- New behavioral equalizer with new will be implemented for 32GT/s, featuring a 3-tap DFE and 2nd-order CTLE
- Raw BER remains at 1E-12
- TXEQ presets will remain the same as PCIe 3.0/4.0
- Backward compatibility with slower speeds still expected
- Expected scope BW is 33GHz but still TBD
- Expected eye height at end of channels with EQ is 10mVpp and eye width is 0.3UI i.e 9.375ps

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Compliance Test

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How does a device get approved by PCI-SIG?

PCIe Compliance Testing for Interoperability

- PCI-SIG holds regular Compliance Workshops to verify individual devices' compliance and interoperability, typically 4x/yr.
- Vendors who desire to be on PCI-SIG Integrators List plan to attend PCI-SIG workshops where they must pass all four electrical tests & 80% of interoperability tests
- Vendors are expected to use PCI-SIG approved test equipment **prior to** workshop testing, to ensure they will pass the workshop electrical tests
- PCIe 3.0 compliance testing conducted at workshops currently, PCIe 4.0 "FYI"

PCIE Electrical PHY Compliance Tests
Transmitter Testing
Receiver Jitter Tolerance Testing
Tx/Rx Link Equalization Testing
PLL Loop Bandwidth Testing

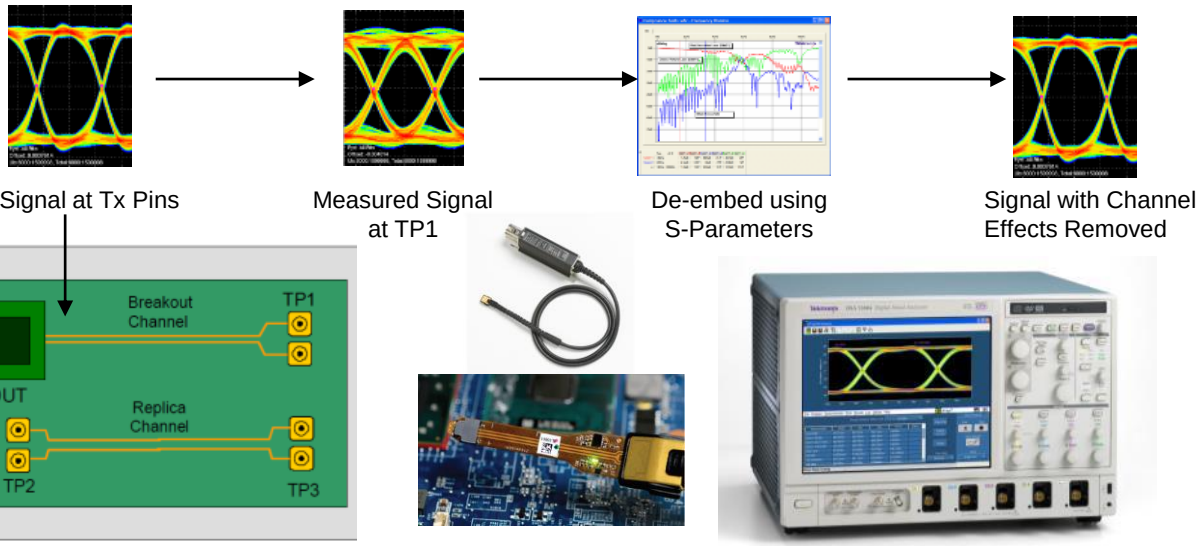
For more details visit PCI Compliance program:
http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library#electrical30

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How Can I Perform Base Tx Testing?

Silicon Level

- Base Specification Measurements are defined at the pins of the transmitter, where signal access at the pins is often not possible
- De-embedding is required to see what the signal looks like at the pins of the TX, without the added effects of the channel, and is challenging
- S-Parameters are acquired on the replica channel
- Measurement at TX pins can also be enabled by high fidelity probes
- PCI-SIG Compliance testing does not cover the Base Specification

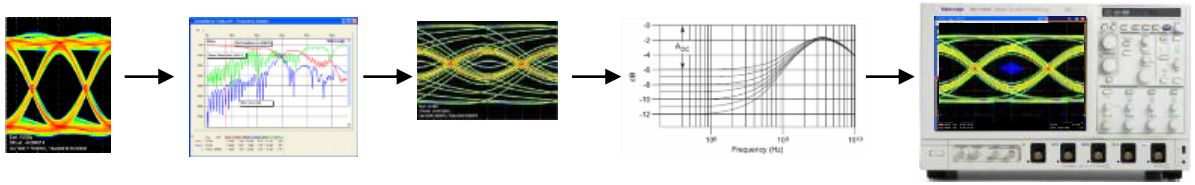


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How Can I Perform CEM Tx Testing?

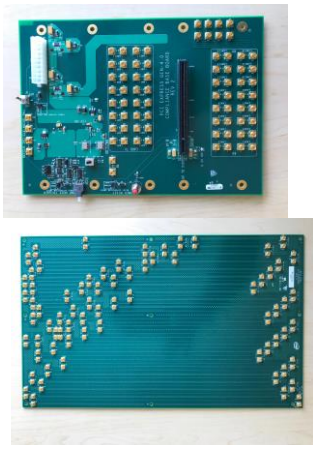
Add-in Card and System Level

- CEM Specification Measurements are defined at the slicer of a receiver, where signal access is not possible
- Embedding of the compliance channel and package, as well as application of the behavioral equalizer is challenging to perform correctly
- Embedding and calculation from measurements is done by SigTest for PCI-SIG compliance testing. Custom software like DPOJET can do similar for unofficial lab testing
- PCI-SIG compliance testing is based on the CEM specification



Signal Acquired from Compliance Board | Embed Compliance Channel and Package | Closed Eye due to the Channel | Apply CTLE + DFE | Open Eye for Measurements

16GT/s CEM Fixtures (Preliminary)



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Receiver Test Fundamentals

Protocol Awareness

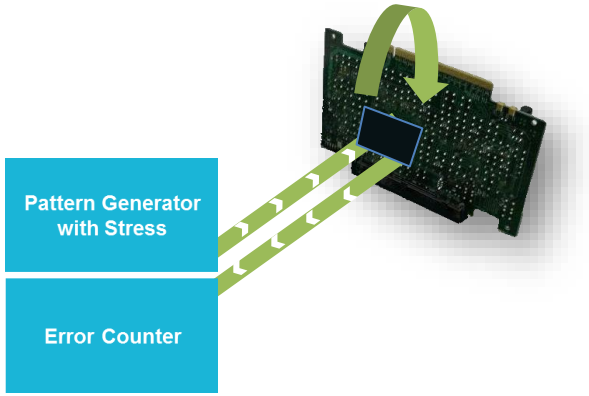
1. Putting device into loopback
2. Performing link equalization

Need Standard Automated Solutions for PCIe 3.0 and 4.0

3. Easy setup of impaired signal
4. Auto calibration of stress impairments
5. Making accurate and repeatable BER measurements

Go Beyond Compliance

6. Root-causing factors leading to bit-error or link training problems



ERROR BIT LOCATION	EXPECTED BIT
200,457	0
1,247,356	1
1,447,890	0
3,885,245	0
4,001,876	1
8,233,191	0
...	

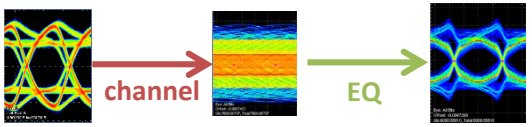
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PCIe Test Challenges

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New Challenges for PCIe 4.0 and Beyond

- Repeater IC's increasingly important to improve signal integrity
 - Increasingly lossy channels and increasingly data rates (**-28dB** for PCIe 4.0 CEM and **-36dB** for PCIe 5.0)
 - **Need to open eye at end of the channel!**
 - Different types of repeater IC's used:
 - *Redriver—no clock-data recovery (CDR)*
 - *Clock-synchronous retimer—has CDR, clocks data to recovered clock*
 - *Clock-compensating retimer—has CDR, clocks data to ref clock*
 - Repeaters include some combination of SERDES, CDR, and CTLE/DFE equalization capability to open eye after lossy channel
 - *CTLE = continuous time linear equalization*
 - *DFE = decision feedback equalizer*



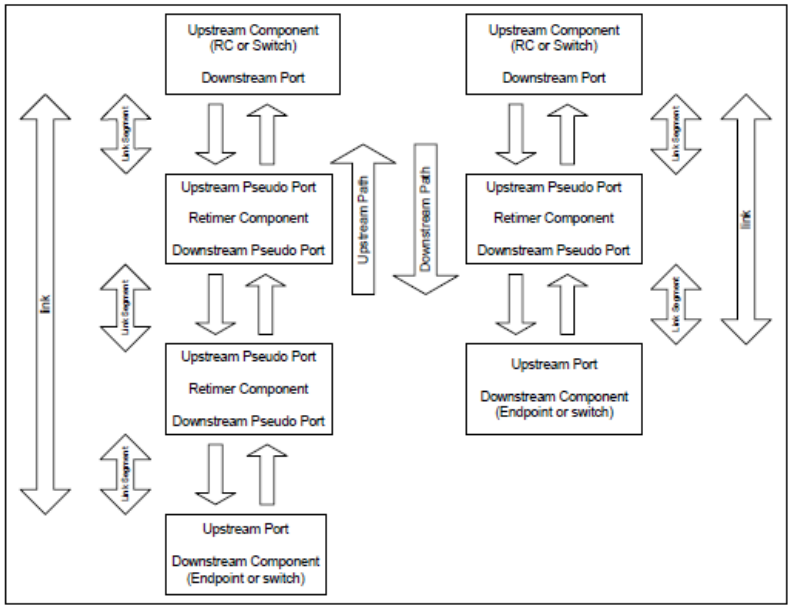
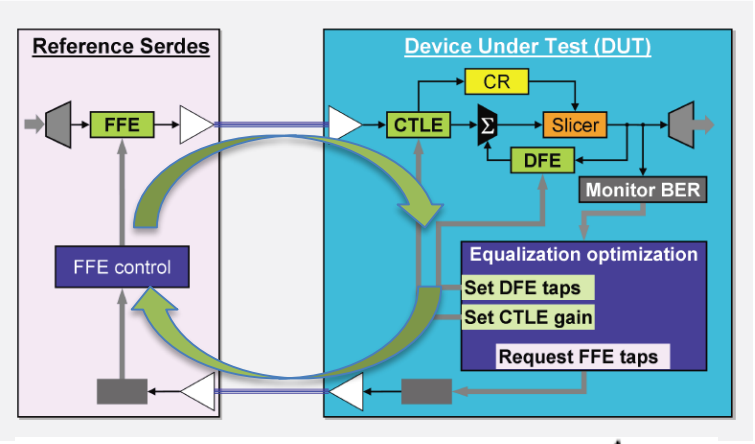


Figure 4-36 Supported Retimer Topologies

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New Challenges for PCIe 4.0 and Beyond

- Entire link (including repeaters) requires link training capability
 - Adaptive, optimizing equalization that requires coordination of Tx and Rx for each link at power up and recovery
 - Precise orchestration of FFE, CTLE, CR, slicer, and DFE functionality is essential,
 - Data stream/protocol management (scrambling, sequencing, encoding test patterns)
- NRZ (non-return to zero) symbol decoders/bit slicers with 15mVpp sensitivity for PCIe 4.0 and 10mVpp sensitivity for 32GT/s

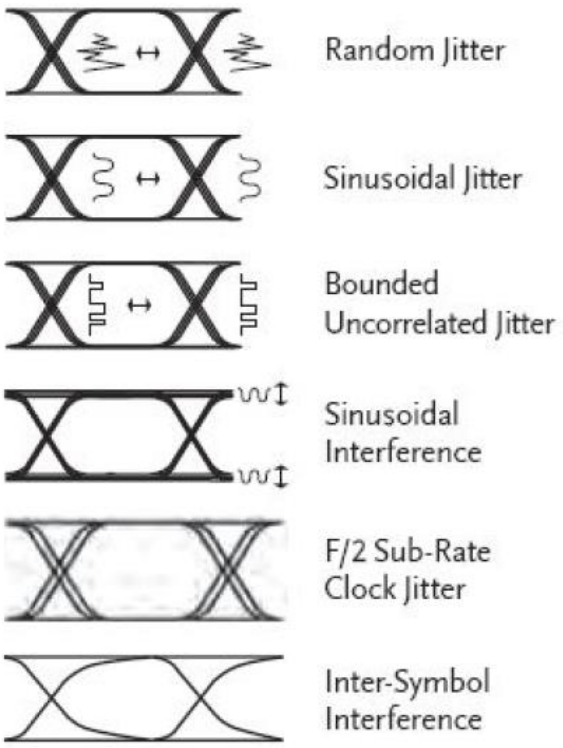




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New Challenges for PCIe 4.0 and Beyond

- Receiver margin testing requires calibrated insertion of various stresses for worst-case compliance testing:
 - Inter-Symbol Interference (ISI)
 - Random Jitter (RJ),
 - Sinusoidal Jitter (SJ),
 - Common-mode/Differential mode Interference (CMI/DMI)
- Reference receiver models assist in calibrating compliance test conditions (eg Seasim/SigTest)
 - Models include the transmitted signal, applied stresses, and channel response to the receiver input pins

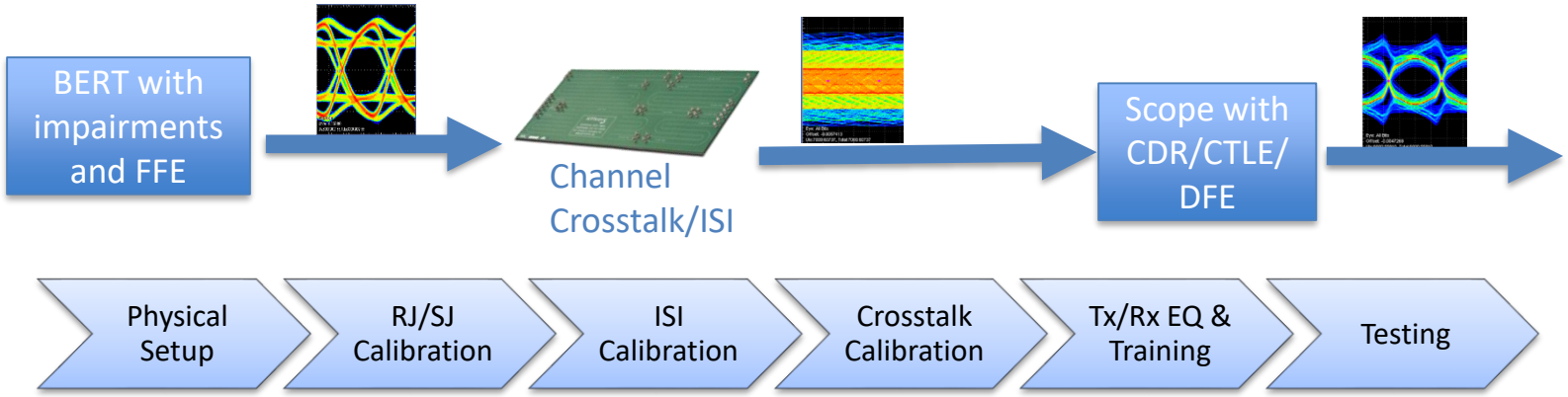


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How to Address New PCIe 4.0 and Beyond Challenges?

PHY and Protocol-Aware Test and Debug

- Need fully integrated test system, including HW and SW solutions
 - Reliably put device under test into loopback mode
 - Facilitate link equalization training to optimize the channel, including built-in TXEQ and RXEQ optimization
 - Calibrate and sweep full suite of impairments (ISI, RJ, DMSI, CMI)
 - Debug DUT-specific problems with BER, FEC, and link training
- Solution must cover multiple standards and spec generations (eg PCIe 3.0-4.0, etc)



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PCIe Test Solutions

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Tektronix Transmitter Test Solution for PCIe at 32GT/s



Instrument Needed	
8GT/s:	DPO71254C Minimum Bandwidth: 12.5GHz
16GT/s:	DPO72504DX or DPO73304SX Minimum Bandwidth: 25GHz
32GT/s:	DPO73304DX or DPO73304SX Minimum Bandwidth: 33GHz**

SX Scope utilizes patented ATI (asynchronous time interleaving) technology improving noise floor performance at 32GT/s

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Tektronix Receiver Test Solution for PCIe at 32GT/s

- **Simplified testing**
 - Full-rate output and built-in calibrated impairments up to **32GT/s**
 - Reference clock multiplication and interference generation
 - Protocol Awareness with pattern sequencer
- **One instrument for PCIe 3.0 and beyond Rx testing needs**
 - Automates running of compliance tests
 - PCIe 3.0 and 4.0
 - Automated calibration wizard
- **Sophisticated error analysis tools**
 - Pattern Sensitivity
 - Error Free Interval Tool
 - Forward error correction emulation

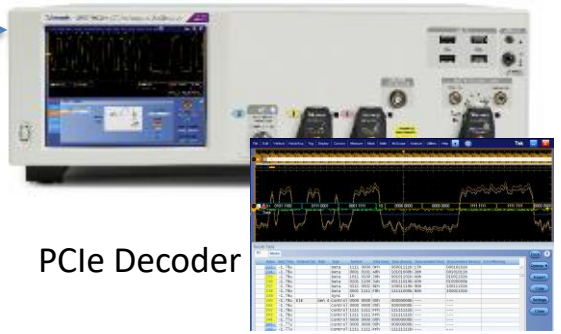


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PCIe Link EQ Testing Process



Protocol-based trigger



PCIe Decoder

< 500ns



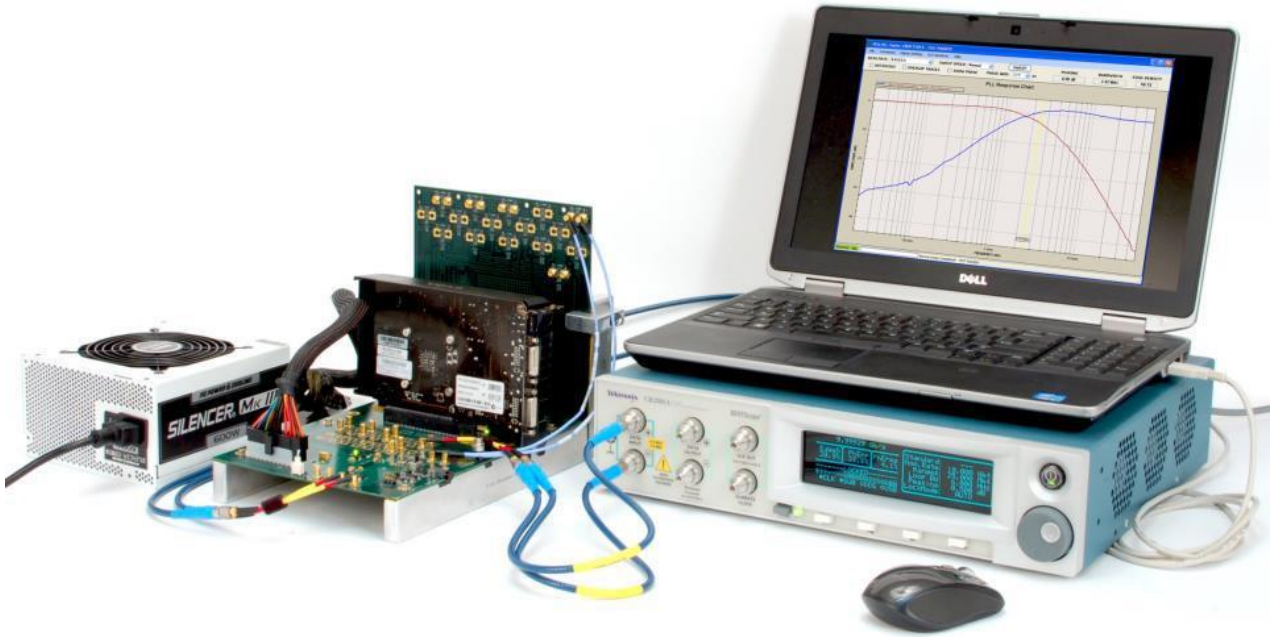
- BERT sends trigger to scope based on customizable protocol message match
- BERT and DUT negotiate through Link EQ by optimizing TxEQ from BSX
- BERT uses LTSSM to train DUT's transmitter
- BERT uses handshaking to put DUT into loopback

- Testing is run at PCIe compliance workshops, debug often required

- Scope decodes PCIe 1.0-4.0 protocol messages
- Scope verifies DUT has actually implemented the preset/EQ that it claims to have done
- DUT must "train up" in speed—8GT/s, & 16GT/s
- Scope verifies handshaking was performed in **<500ns**

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PLL Loop Bandwidth Testing Process Automation



- **Phase modulate reference clock and measure phase error on DUT Tx**
- **≤30 second test time across full sweep range**
- **Full data rate support: 2.5GT/s, 5GT/s, 8GT/s, 16GT/s**
- **Simple two button operation: set data rate, hit “Sweep” button**

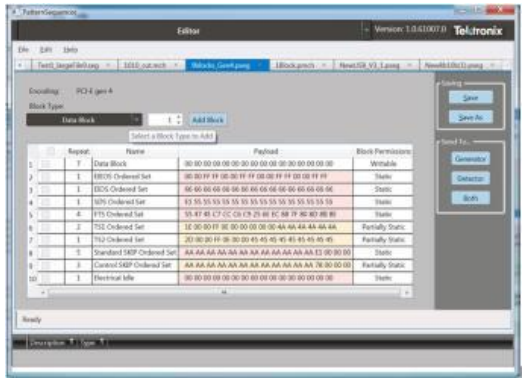
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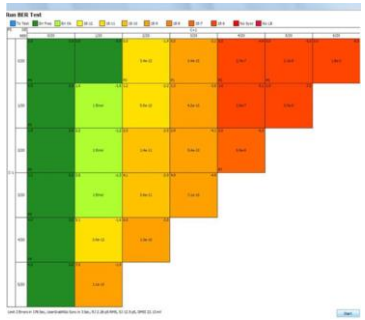
Loopback / Link Training Process

- **User Challenges:**
 - Preparing receiver for test**: reliably putting device under test into loopback mode and completing link equalization training to optimize the channel**
 - Debugging loopback and equalization failures

- **For best debugging, tool should provide:**
 - Compliant link equalization training for PCIe 3.0 and 4.0
 - **Fast (500ns) link training response time**
 - Handshaking support above 16GT/s
 - Auto tuning and optimizing Rx EQ settings via BER map

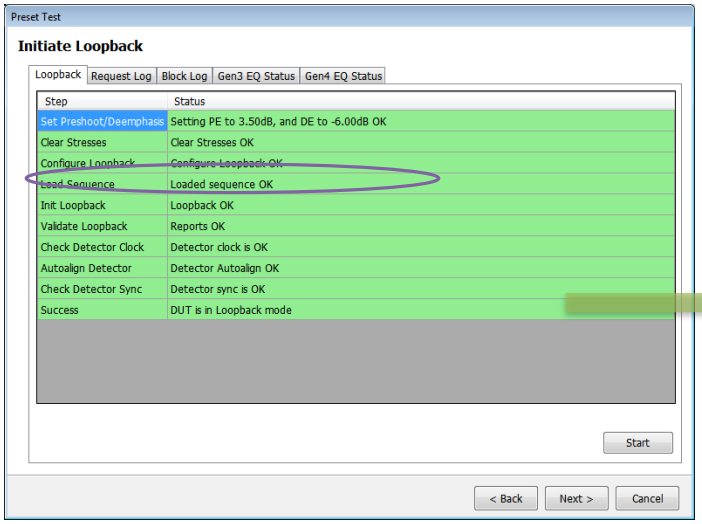


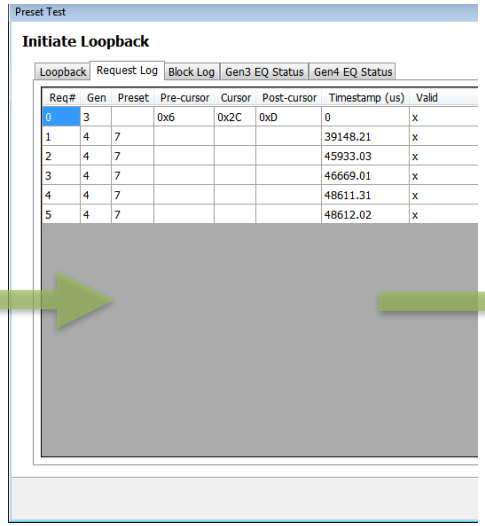


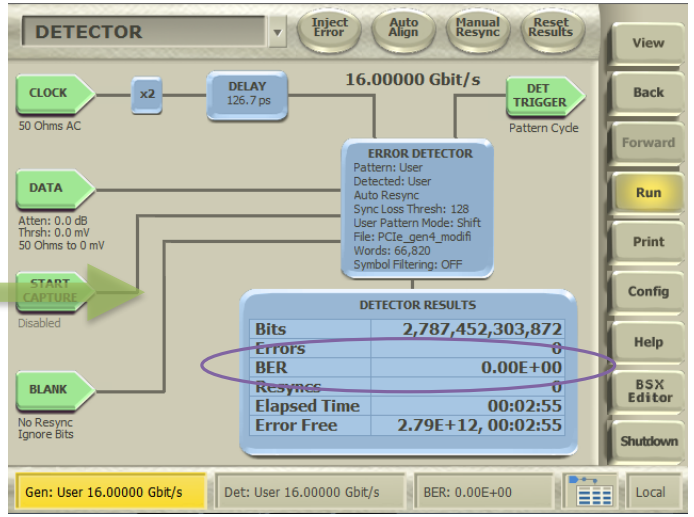


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PCIe 4.0 CEM Handshaking Example







Sequencer Loaded for PCIe Loopback Initiation and Debug

Multiple iterative requests from the DUT for TXEQ tuning

Error Free Operation Achieved!

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Debug Tools

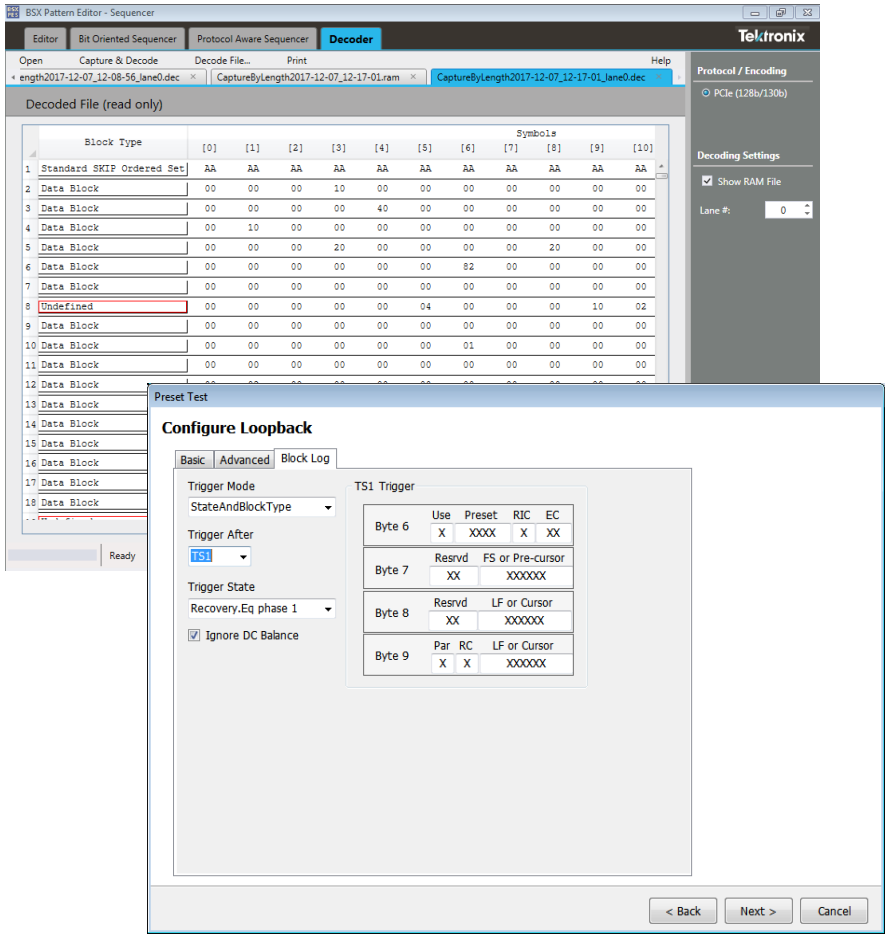
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PCIe Link Training Capture and Decode

Decreases Time and Stress of Troubleshooting by Providing Insights

Key benefits:

- Debug complex training issues in protocol link training between DUT and BERT
- Captures and decodes protocol blocks and displays in searchable event table
- Rx Test application supports flexible triggered capture and decode based on state transition and/or protocol messages

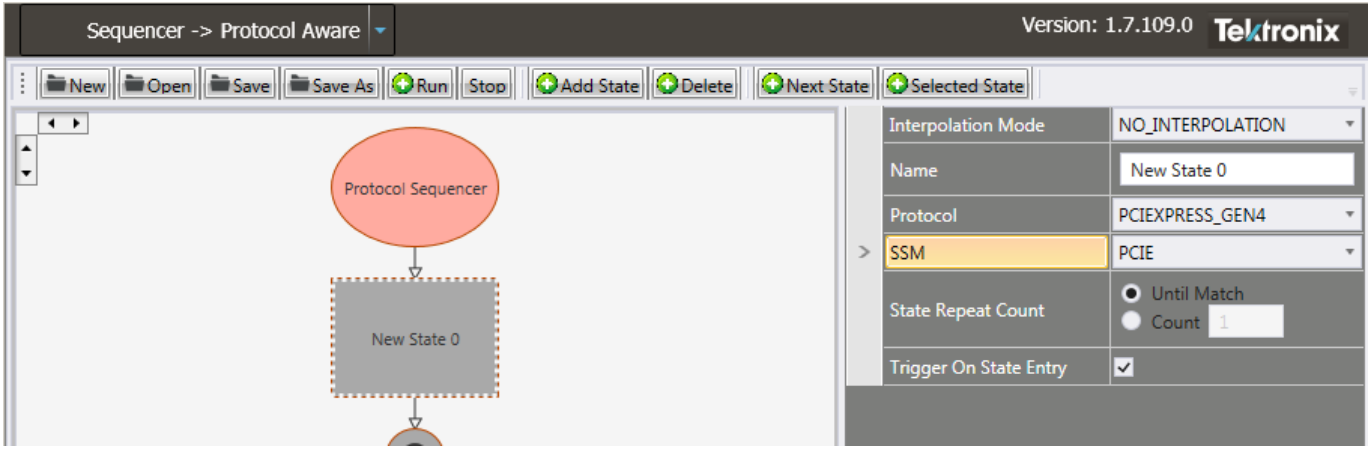


***NEW* PCIe 3.0/4.0 Protocol Capture and Decode**

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PCIe Link Training Sequencer Debug Tools

Decreases Time and Stress of Troubleshooting by Providing Insights



Customizable protocol-aware sequencer

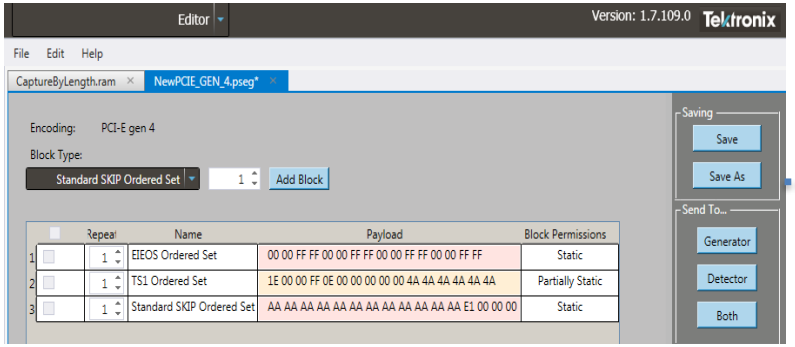
Key Benefits:

- In protocol-aware mode, words are treated as protocol blocks instead of bits
- User can implement standard PCIe link training sequence, or customize using additional blocks (ex. SKP ordered sets, TS1's, or EIEOS to debug)
- User-defined pattern match elements enable customizable handshaking sequences

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PCIe Link Training Match and Trigger Tools

Decreases Time and Stress of Troubleshooting by Providing Insights



Protocol-based trigger



Pattern/protocol match and scope cross-trigger

Key Benefits:

- Using cross-triggering of scope to debug transition timing problems (ie from PCIe 3.0 to 4.0)
- BERT triggering combined with scope protocol decoding provides unprecedented handshaking debug visibility
- Scope protocol decoding of captured waveform provides correlated debug insights

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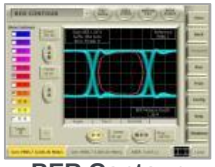
Debugging Rx BER Failures

User Challenge:

- Need more than a bit-error rate (BER) number
- Need to understand factors leading to bit error problems in order to debug issues

BSX Series BERTScope provides:

- "Scope" functionality that complement those of the Tektronix scopes
- Full-featured and easy to use analysis tools
- Eye diagram for quick diagnosis of synchronization and BER failure issues
- Debug challenging signal integrity problems
 - Error Location Analysis
 - Pattern Capture
 - Jitter Map
 - BER Contour
 - FEC Emulation

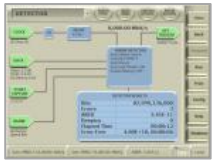

BER Contour


Eye Diagram


Error Location Correlation


FEC Emulation


Jitter Map


BER


Jitter


Jitter Tolerance

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Conclusion

- **PCIe 4.0 and beyond introduces new test calibration and test methodologies, including new fixtures**
- **Evaluation of Rx and Tx compliance testing procedures and tools is now underway**
- **Handshaking for loopback and equalization training is now available**
- **Debugging tools for physical layer and handshaking issues have advanced with the latest generation of Rx and Tx test equipment**

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